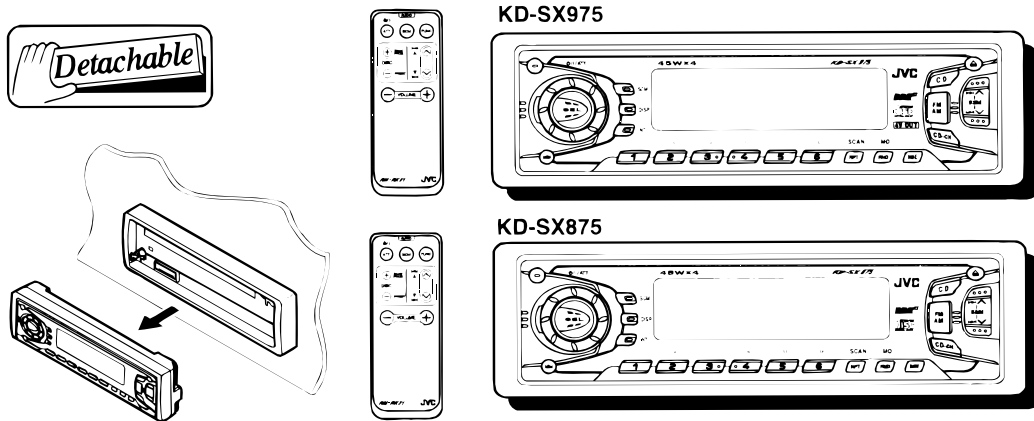


JVC

SERVICE MANUAL

CD RECEIVER

KD-SX975 / KD-SX875



BBE^{II}

**COMPACT
disc
DIGITAL AUDIO**


Area Suffix


U ---- Other Areas

Contents

Safety precaution	1-2	Flow of functional	1-11
Preventing static electricity	1-3	operation unit TOC read	
Location of main parts	1-4	Maintenance of laser pickup	1-13
Disassembly method	1-5	Replacement of laser pickup	1-13
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Safety precaution

 **CAUTION** Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of performing repair of this system.

 **CAUTION** Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.

Preventing static electricity

1. Grounding to prevent damage by static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

2. About the earth processing for the destruction prevention by static electricity

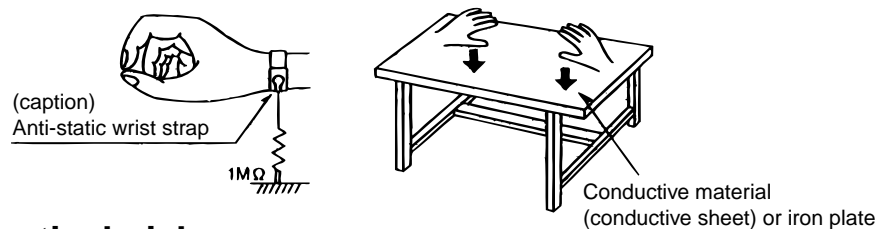
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as CD players. Be careful to use proper grounding in the area where repairs are being performed.

2-1 Ground the workbench

Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

2-2 Ground yourself

Use an anti-static wrist strap to release any static electricity built up in your body.



3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

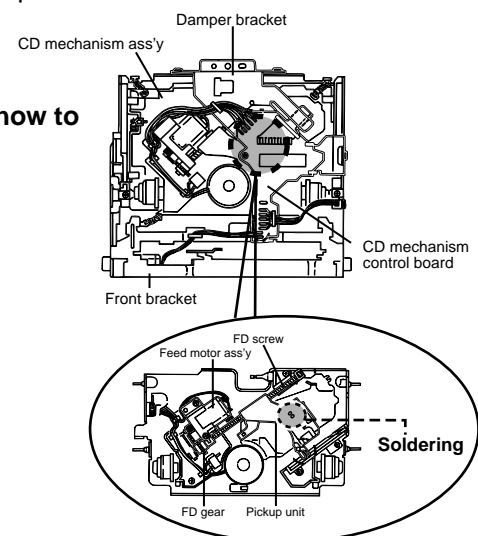
4. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
3. Handle the flexible cable carefully as it may break when subjected to strong force.
4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Attention when traverse unit is decomposed

***Please refer to "Disassembly method" in the text for pick-up and how to detach the substrate.**

1. Solder is put up before the card wire is removed from connector on the CD substrate as shown in Figure.
(When the wire is removed without putting up solder, the CD pick-up assembly might destroy.)
2. Please remove solder after connecting the card wire with when you install picking up in the substrate.

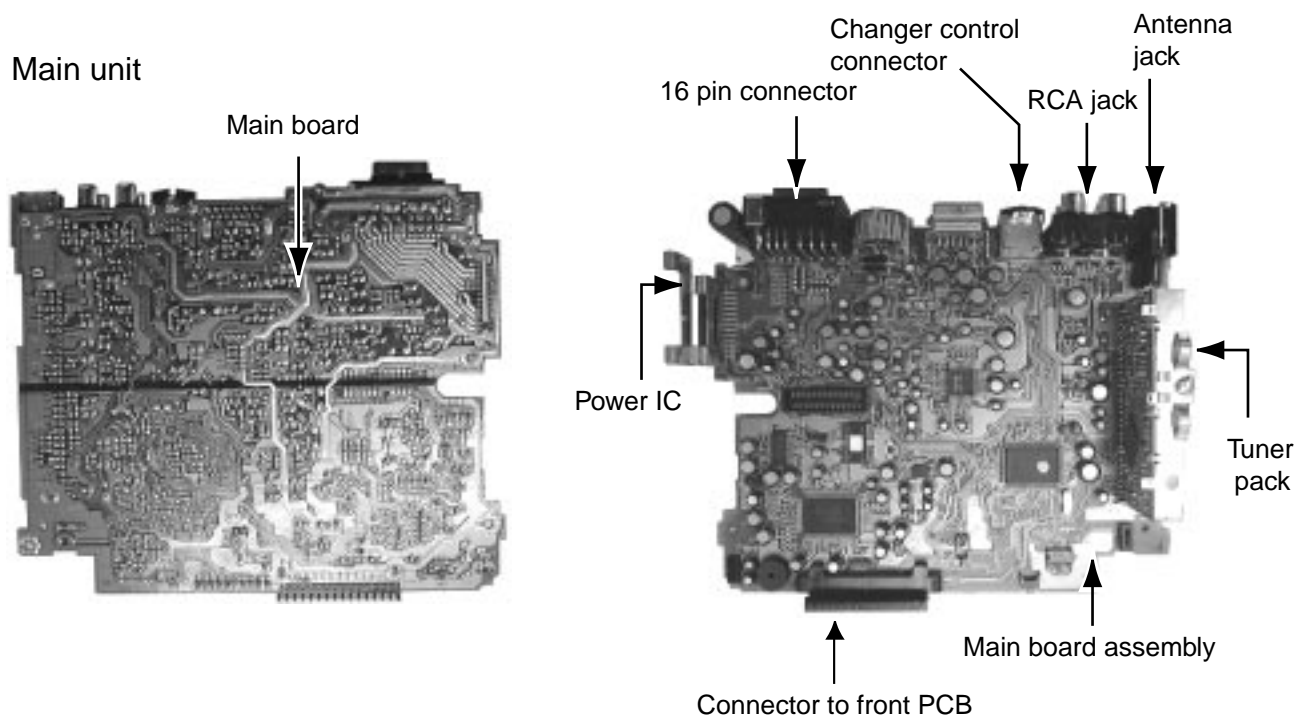


Location of main parts

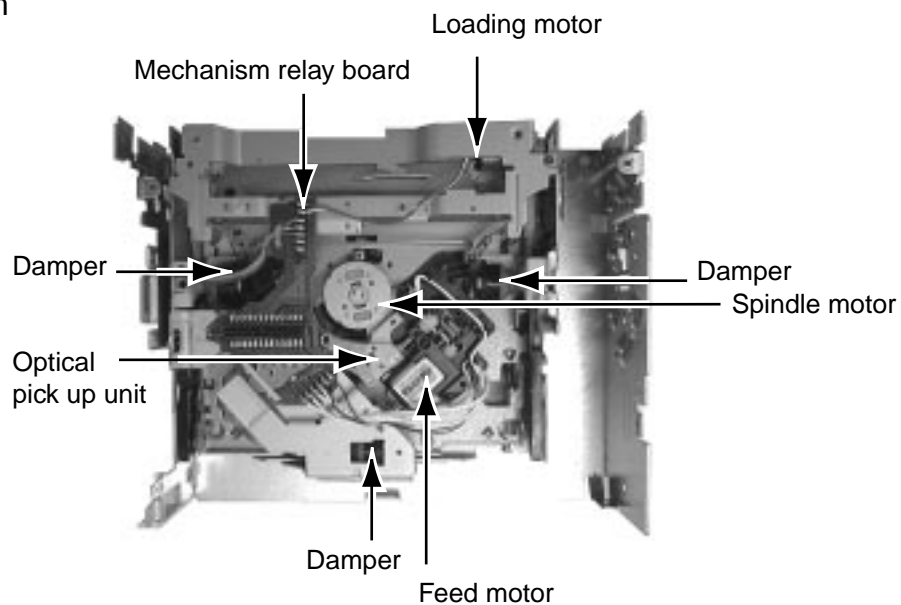
■ Control unit



■ Main unit



■ CD mechanism



Disassembly method

■ Removing the front chassis (See Fig.1)

1. Remove two screws A and insert a screwdriver to the joints a on the side of the front chassis and two joints b on the right side, then detach the front chassis toward the front side.

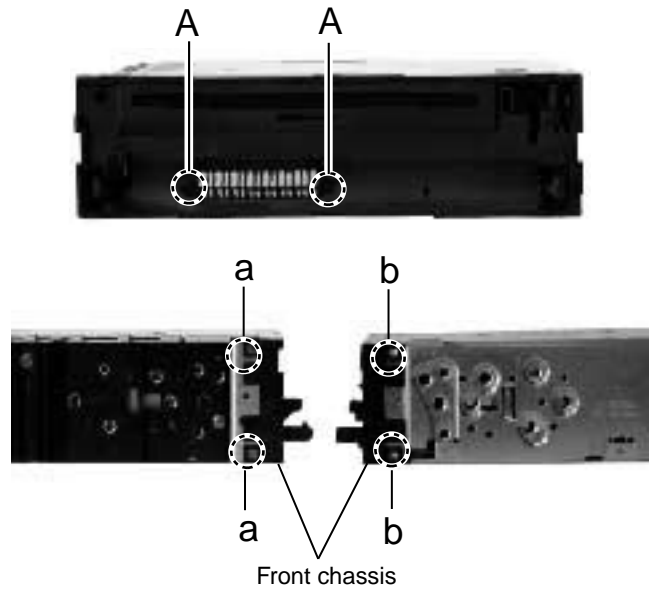


Fig.1

■ Removing the heat sink (See Fig.2)

1. Remove the three screws B attaching the heat sink on the left side of the body, and remove the heat sink.

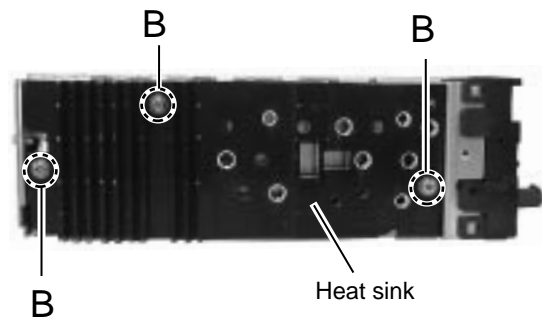


Fig.2

■ Removing the bottom cover (See Fig.3)

1. Turn the body upside down.
2. Insert a screwdriver to the two joints c and two joints d on both sides of the body and the joint e on the back of the body, then detach the bottom cover from the body.

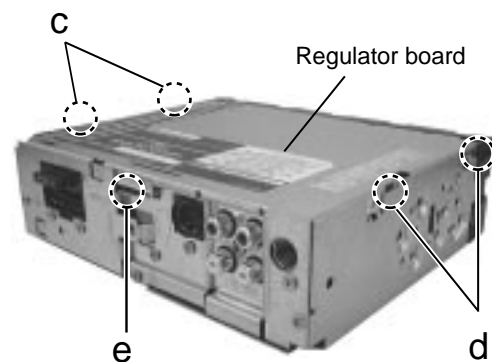


Fig. 3

■ Removing the main amplifier board assembly

(See Fig.4 and 5)

1. Remove the front chassis.
2. Remove the bottom cover.
3. Remove the two screws C attaching the main amplifier board assembly on the bottom of the body.
4. Remove the three screws D attaching the main amplifier board assembly on the back of the body.
5. Disconnect connector CN501 on the main amplifier board assembly from the CD mechanism assembly.

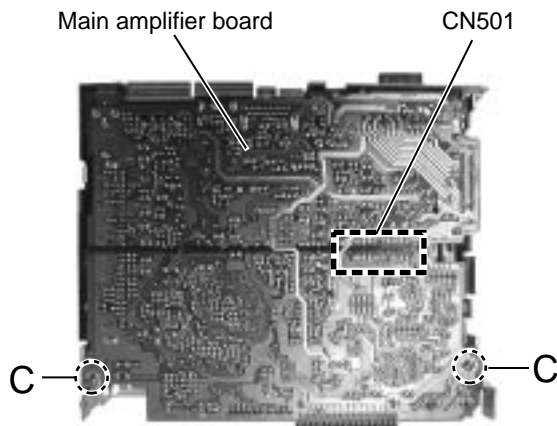


Fig.4

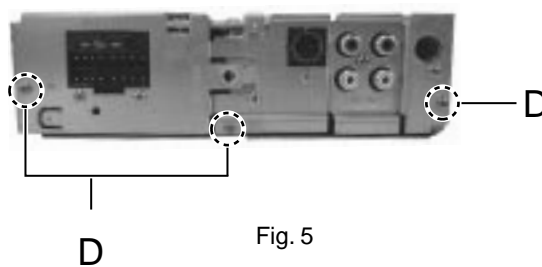


Fig. 5

■ Removing the CD mechanism assembly

(See Fig.6)

1. Remove the front chassis.
2. Remove the bottom cover.
3. Remove the main amplifier board assembly.
4. Remove the three screws E attaching the CD mechanism assembly from the top cover.

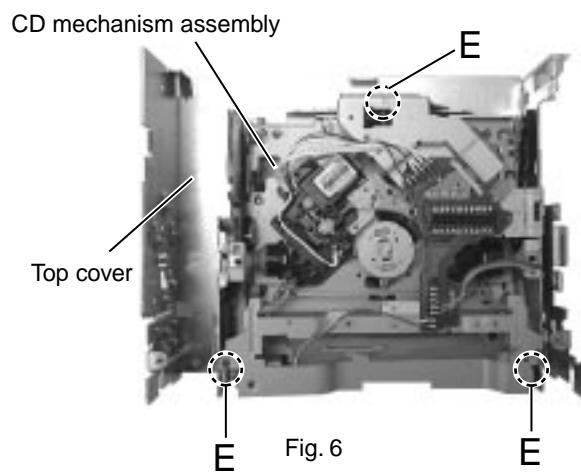


Fig. 6

■ Removing the control switch board

(See Fig.7 and 8)

1. Remove the front chassis.
2. Remove the four screws F attaching the rear cover on the back of the front panel unit.
3. Remove the control switch board from the front panel unit.

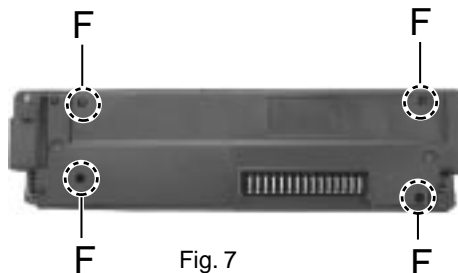


Fig. 7

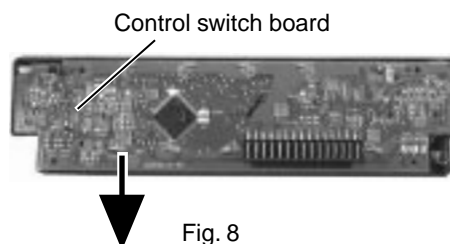


Fig. 8

<CD mechanism section>

■ Removing the CD mechanism control board (See Fig.1 and 2)

1. Unsolder the part **a** and **b** on the CD mechanism control board.
2. Remove the stator fixing the CD mechanism control board and the damper bracket (To remove the stator smoothly, pick up the center part).
3. Remove the screw **A** attaching the CD mechanism control board.
4. Remove the CD mechanism control board in the direction of the arrow while releasing it from the two damper bracket slots **d** and the front bracket slot **e**.
5. Disconnect the flexible wire from connector on the pickup unit.

ATTENTION: Turn the FD gear in the direction of the arrow to move the entire pickup unit to the appropriate position where the flexible wire of the CD mechanism unit can be disconnected easily.
(Refer to Fig.2)

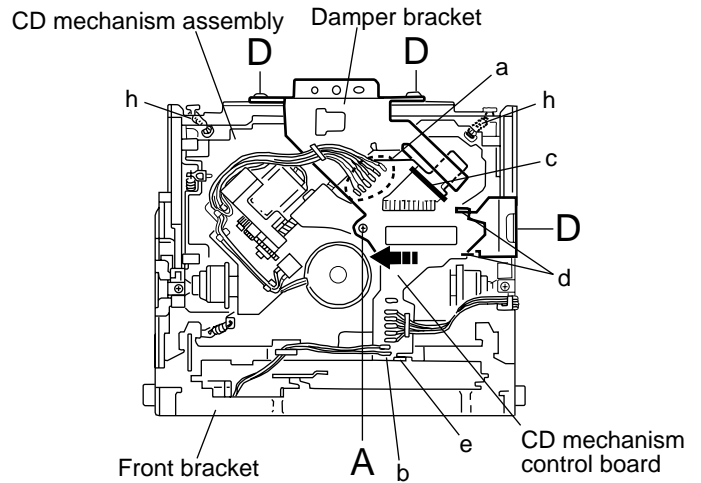


Fig.1

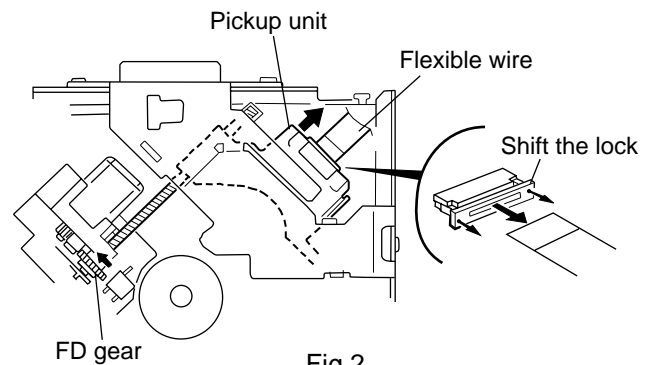


Fig.2

■ Removing the loading motor (See Fig.3 to 5)

- Prior to performing the following procedure, remove the CD mechanism control board.
1. Remove the two springs **f** attaching the CD mechanism assembly and the front bracket.
 2. Remove the two screws **B** and the front bracket while pulling the flame outward.
 3. Remove the belt and the screw **C** from the loading motor.

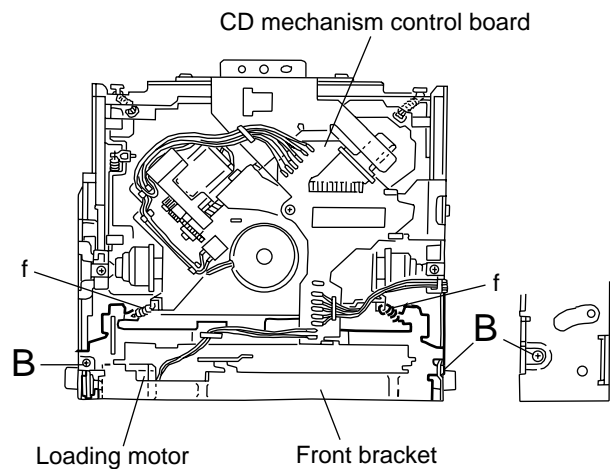


Fig.3

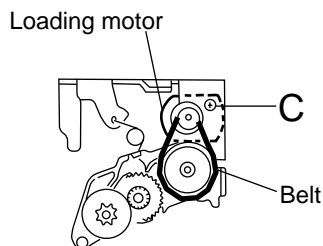


Fig.5

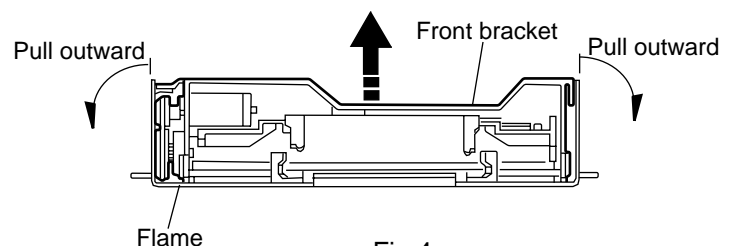


Fig.4

**■ Removing the CD mechanism assembly
(See Fig.1, 6 to 9)**

- Prior to performing the following procedure, remove the CD mechanism control board and the front bracket (loading motor).
1. Remove the three screws **D** and the damper bracket.
 2. Raise the both sides fix arms and move the fix plates in the direction of the arrow to place the four shafts **g** as shown in Fig.8 and 9.
 3. Remove the CD mechanism assembly and the two springs **h** attaching the flame.
 4. Remove the two screws **E** and both sides rear damper brackets from the dampers. Detach the CD mechanism assembly from the left side to the right side.

ATTENTION: The CD mechanism assembly can be removed if only the rear damper bracket on the left side is removed.

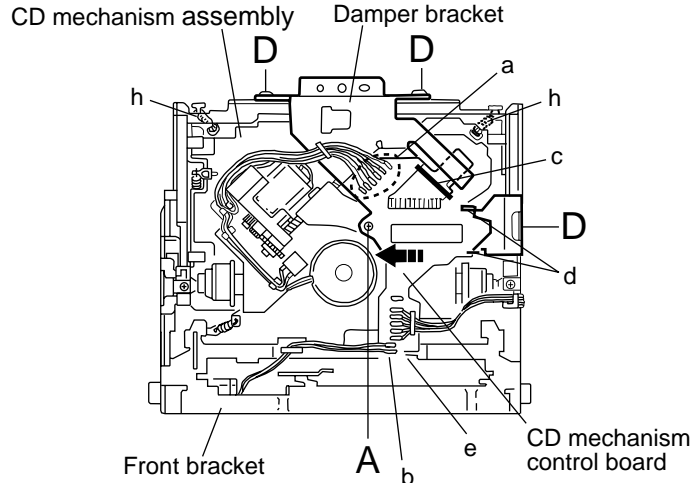


Fig.1

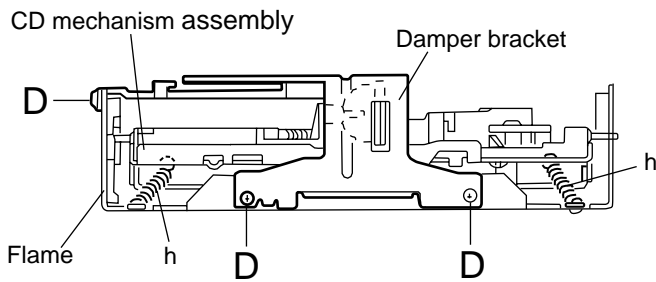


Fig.6

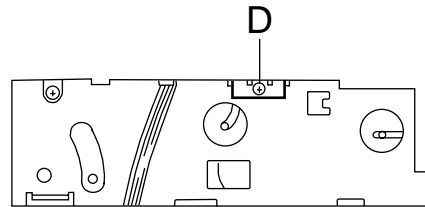


Fig.7

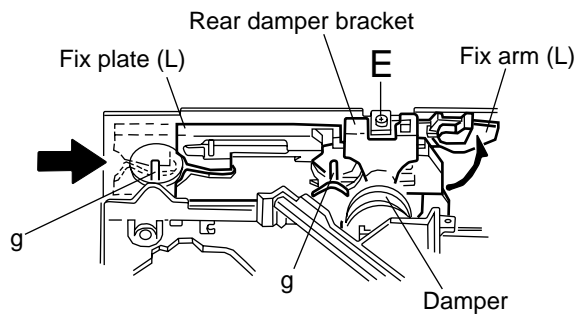


Fig.8

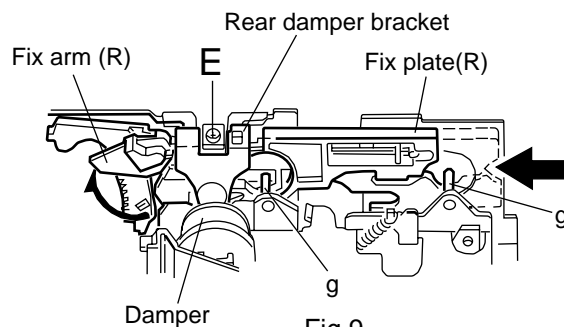


Fig.9

■ Removing the feed motor assembly (See Fig.10)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor) and the CD mechanism assembly.
1. Remove the two screws **F** and the feed motor assembly.

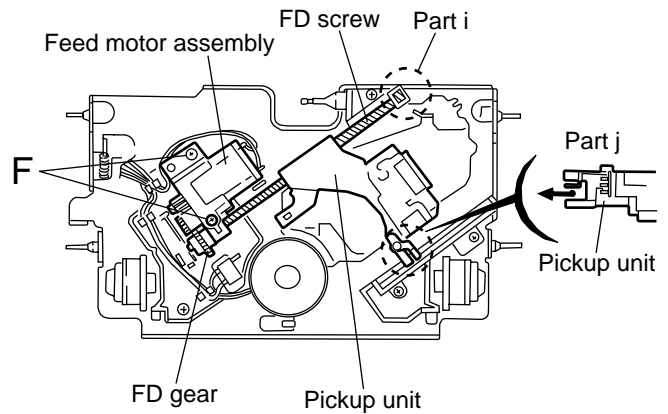


Fig.10

■ Removing the pickup unit (See Fig.10 and 11)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.
1. Detach the FD gear part of the pickup unit upward. Then remove the pickup unit while pulling out the part i of the FD screw.

ATTENTION: When reattaching the pickup unit, reattach the part **j** of the pickup unit, then the part **i** of the FD screw.

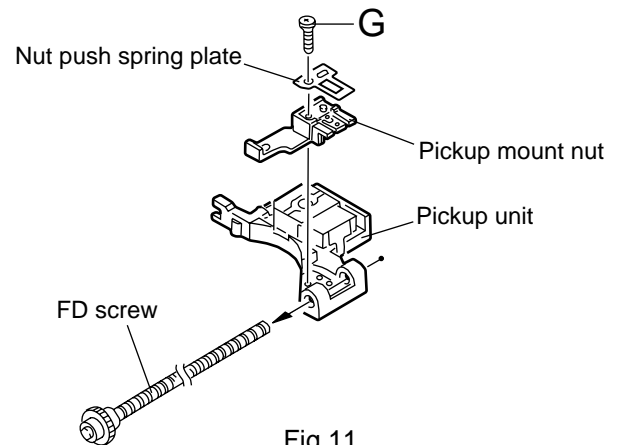


Fig.11

2. Remove the screw **G** attaching the nut push spring plate and the pickup mount nut from the pickup unit. Pull out the FD screw.

■ Removing the spindle motor (See Fig.12 and 13)

- Prior to performing the following procedure, remove the CD mechanism control board, the front bracket (loading motor), the CD mechanism assembly and the feed motor assembly.

1. Turn up the CD mechanism assembly and remove the two springs **k** on both sides of the clamber arms. Open the clamber arm upward.
2. Turn the turn table, and remove the two screws **H** and the spindle motor.

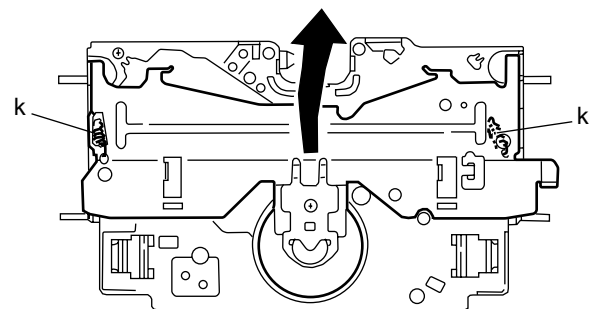


Fig.12

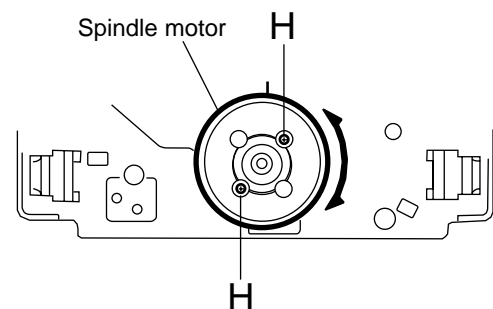


Fig.13

Adjustment method

■ Test instruments required adjustment

1. Digital oscilloscope (100MHz)
2. AM Standard signal generator
3. FM Standard signal generator
4. Stereo modulator
5. Electric voltmeter
6. Digital tester
7. Tracking offset meter
8. Test Disc JVC : CTS-1000
9. Extension cable for check
EXTGS004-26P

■ Standard volume position

Balance and Bass & Treble volume : Indication "0"
BBE:OFF

■ Frequency Band

FM 1 – 3 87.5MHz – 108.0MHz
MW 531kHz – 1602kHz

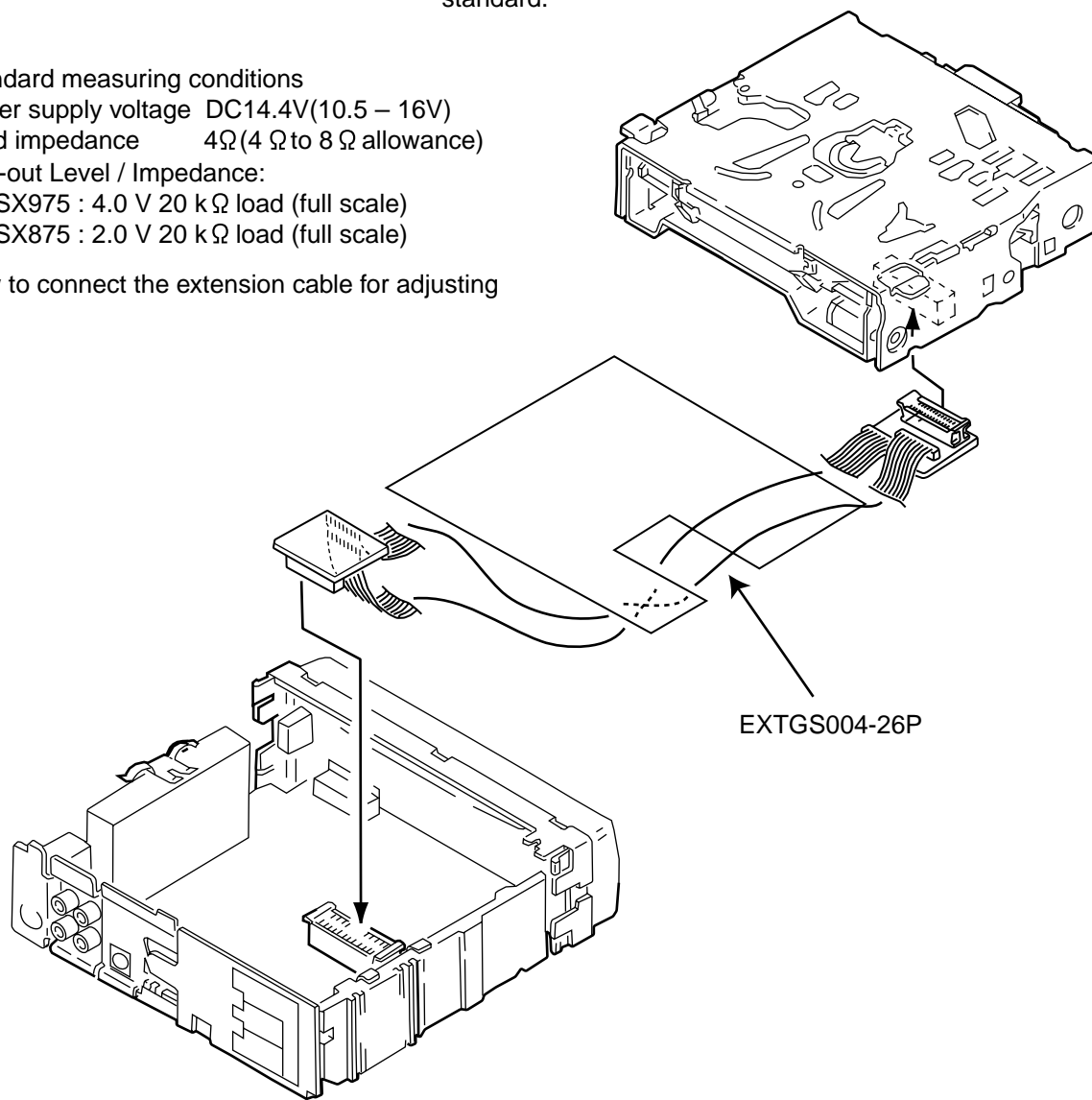
■ Dummy load

Exclusive dummy load should be used for AM, and FM.
For FM dummy load, there is a loss of 6dB between SSG output and antenna input. The loss of 6dB need not be considered since direct reading of figures are applied in this working standard.

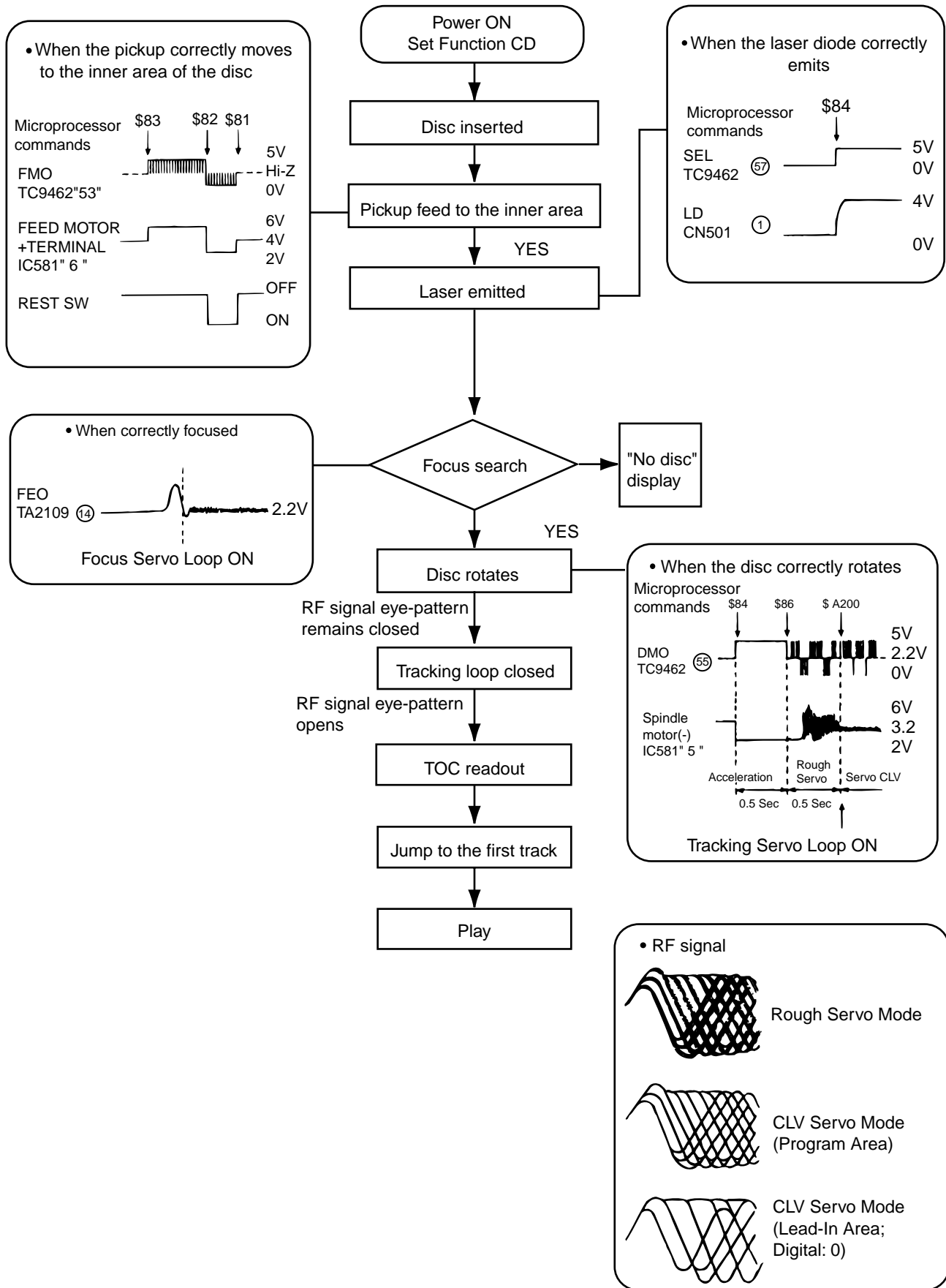
■ Standard measuring conditions

Power supply voltage DC14.4V(10.5 – 16V)
Load impedance 4Ω (4 Ω to 8 Ω allowance)
Line-out Level / Impedance:
KD-SX975 : 4.0 V 20 k Ω load (full scale)
KD-SX875 : 2.0 V 20 k Ω load (full scale)

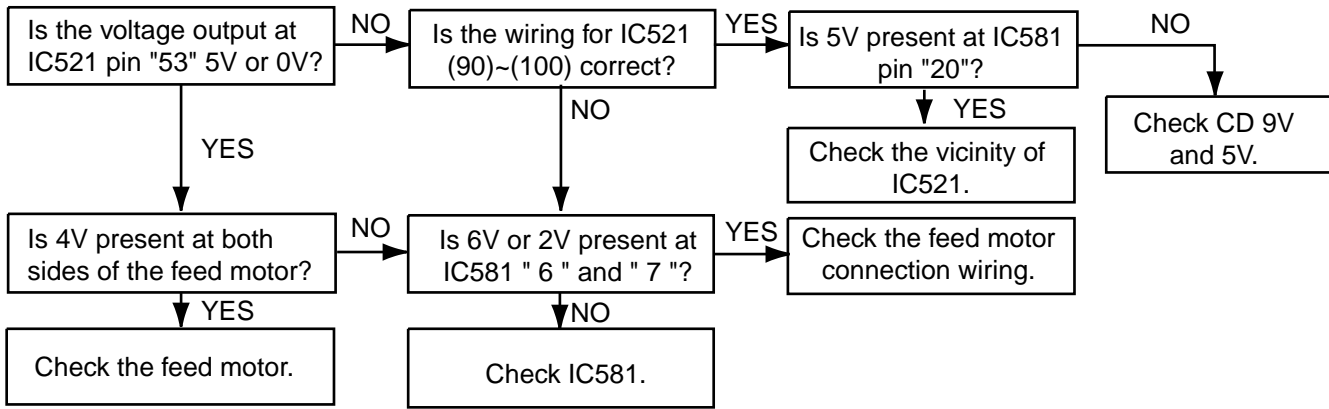
■ How to connect the extension cable for adjusting



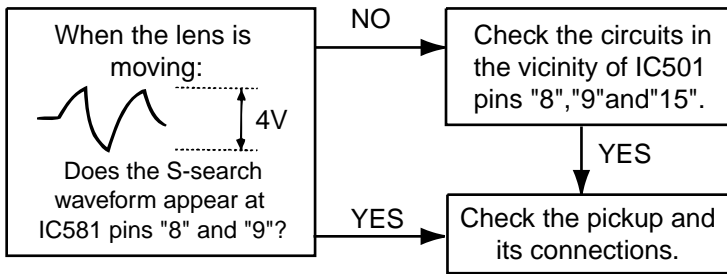
Flow of functional operation unit TOC read



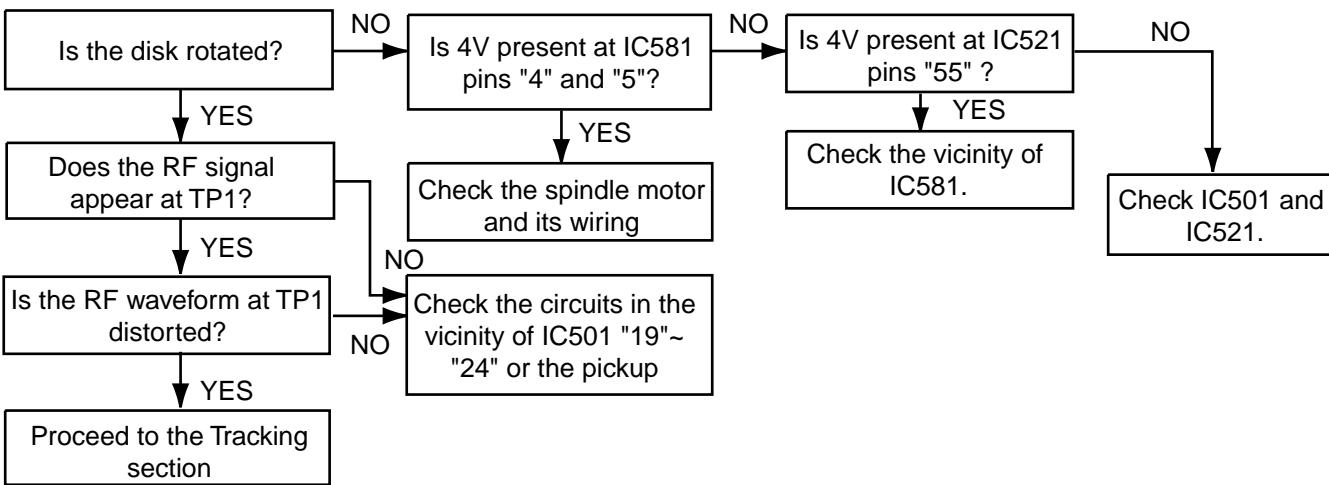
Feed section



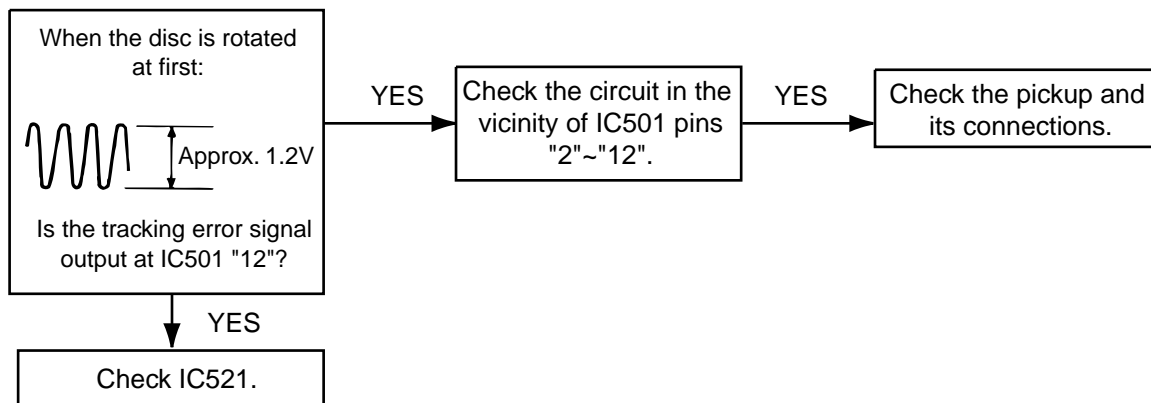
Focus section



Spindle section

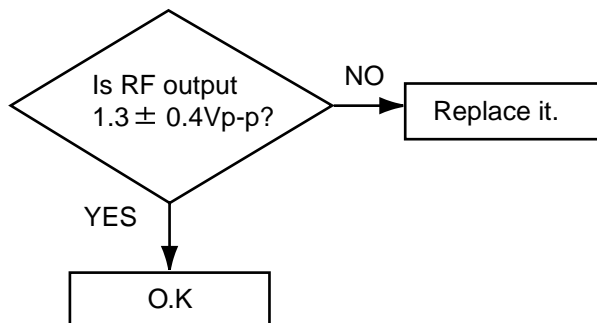


Tracking section



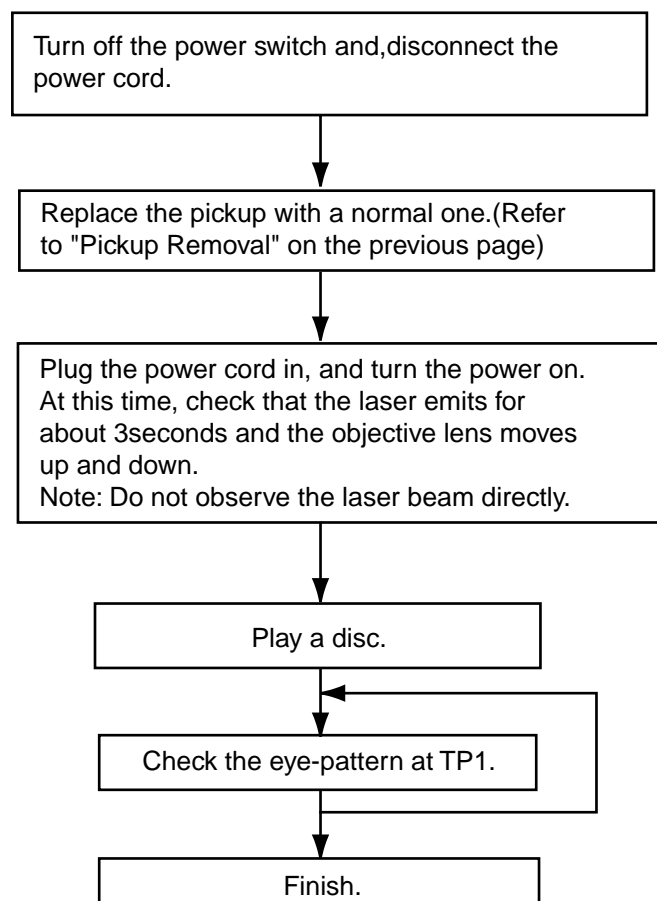
Maintenance of laser pickup

- (1) Cleaning the pick up lens
Before you replace the pick up, please try to clean the lens with a alcohol soaked cotton swab.
- (2) Life of the laser diode
When the life of the laser diode has expired, the following symptoms will appear.
 - (1) The level of RF output (EFM output: amplitude of eye pattern) will be low.



- (3) Semi-fixed resistor on the APC PC board
The semi-fixed resistor on the APC printed circuit board which is attached to the pickup is used to adjust the laser power. Since this adjustment should be performed to match the characteristics of the whole optical block, do not touch the semi-fixed resistor.
If the laser power is lower than the specified value, the laser diode is almost worn out, and the laser pickup should be replaced.
If the semi-fixed resistor is adjusted while the pickup is functioning normally, the laser pickup may be damaged due to excessive current.

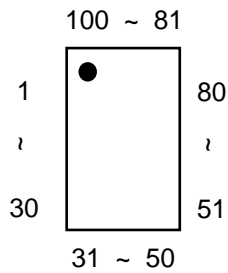
Replacement of laser pickup



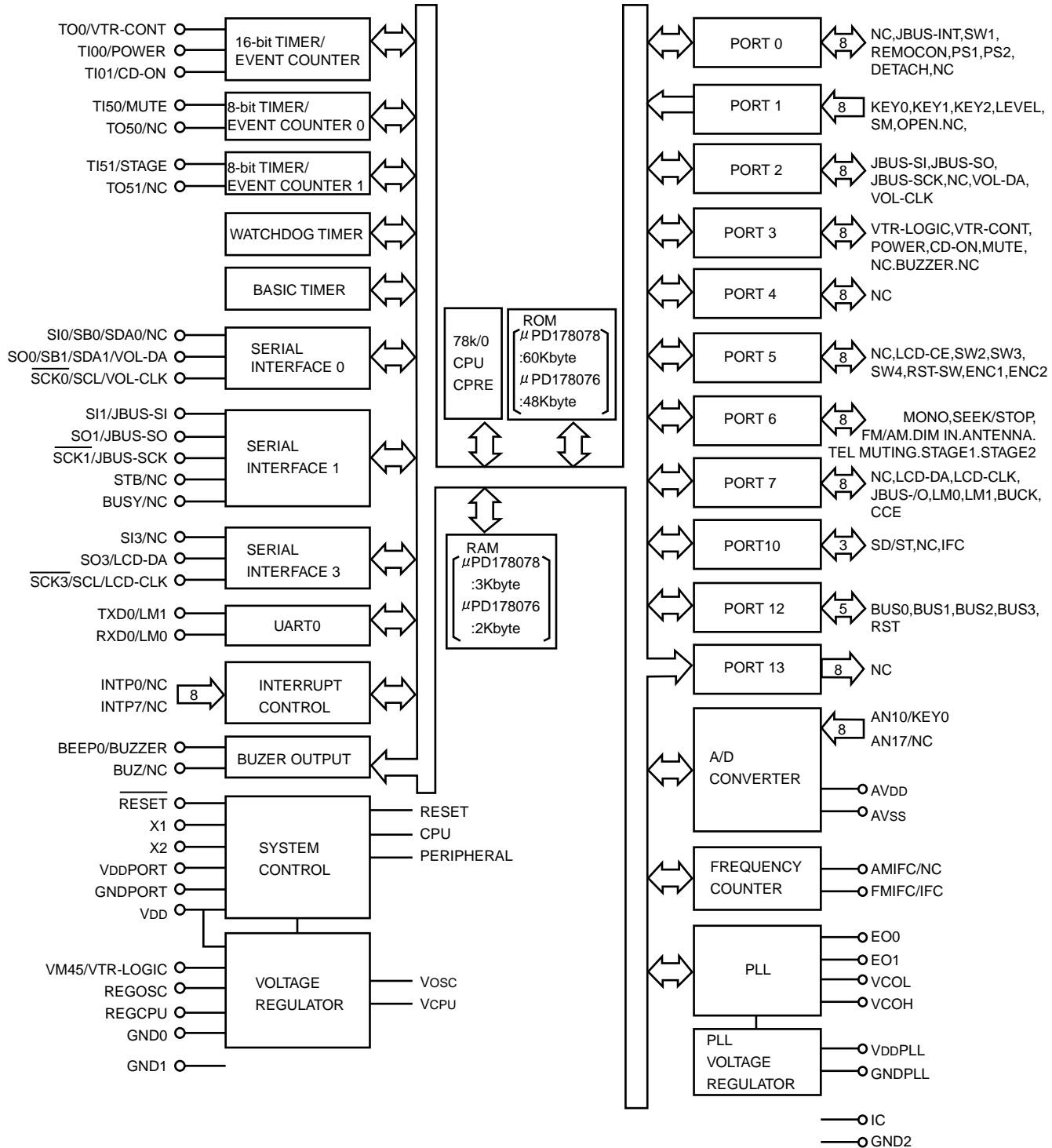
Description of major ICs

■ UPD178078GF-543 (IC701): SYSTEM CPU

1. Terminal layout



2. Block diagram



3.Pin function

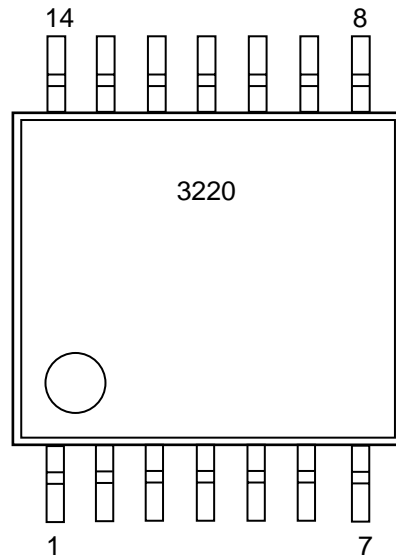
UPD178078GF(1/2)

Pin NO.	Symbol	I/O	FUNCTION
1	NC	-	Non connection
2	JBUS-INT	I	JVC BUS COMMUNICATION LINE
3	JBUS-SI	I	JVC BUS COMMUNICATION LINE
4	JBUS-SO	O	JVC BUS COMMUNICATION LINE
5	JBUS-SCK	O	JVC BUS COMMUNICATION LINE
6	NC	-	Non connection
7	NC	-	Non connection
8	NC	-	Non connection
9	VOL-DA	O	VOL IC COMMUNICATION LINE
10	VOL-CLK	O	VOL IC COMMUNICATION LINE
11	NC	-	Non connection
12	LCD-DA	O	CD DRIVER COMMUNICATION LINE
13	LCD-CLK	O	LCD DRIVER COMMUNICATION LINE
14	JBUS-I/O	O	JVC BUS OUTPUT SELECT
15	NC	-	Non connection
16	LCD-CE	O	LCD DRIVER COMMUNICATION LINE
17	SW2	I	CD MECHA SW
18	SW3	I	CD MECHA SW
19	SW4	I	CD MECHA SW
20	RST-SW	I	TRAVERSE MECHA REST SW
21	ENC1	I	ENCODER INPUT
22	ENC2	I	ENCORDER INPUT
23	KEY0	I	KEY INPUT
24	KEY1	I	KEY INPUT
25	KEY2	I	KEY INPUT
26	LEVEL	I	AUDIO LEVEL INPUT
27	AVDD	-	-
28	SM	I	SIGNAL LEVEL METER INPUT
29	OPEN	I	DOOR OPEN DATECTION
30	NC	-	Non connection
31	NC	-	-
32	AVSS	-	-
33	REGCPU	-	-
34	VDD	-	-
35	REGOSC	-	SYSTEM CLOCK
36	X2	I	SYSTEM CLOCK
37	X1	-	-
38	GND	-	-
39	SD/ST	I	STATION DETECTOR & STERO IND
40	GND2	-	Non connection
41	NC	-	IF COUNT INPUT
42	IFC	I	-
43	VDDPLL	-	FM,AM OSC INPUT
44	OSC-INPUT	I	Non connection
45	NC	-	-
46	GNDPLL	-	PLL ERROR OUTPUT FOR AM
47	AME0	O	PLL ERROR OUTPUT FOR FM
48	FME0	O	SETTING TO WRITE FOR FLASH
49	ICVPP	-	SYSTEM RESET
50	RESET	I	SYSTEM RESET

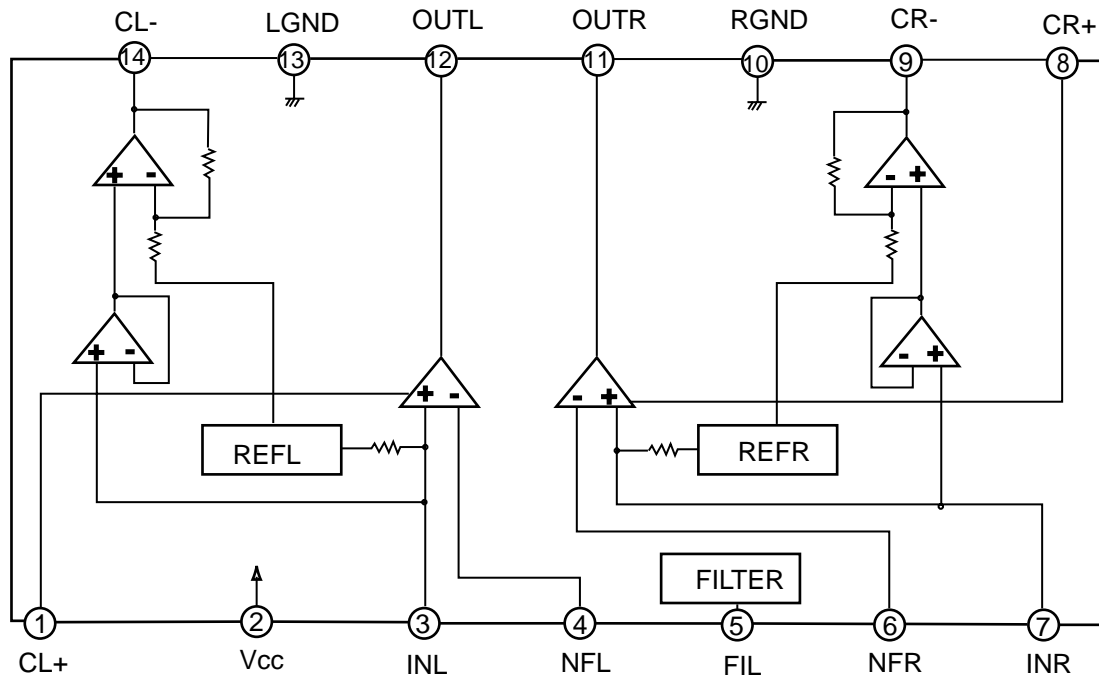
Pin NO.	Symbol	I/O	FUNCTION
51	SW1	I	CD MECHA SW
52	REMOCON	I	REMOCON INPUT
53	VTR-LOGIC	-	Non connection
54	VTR-CONT	-	Non connection
55	POWER	O	POWER CONT.
56	CD-ON	O	CD POWER CONT.
57	MUTE	O	MUTE CONT
58	NC	-	Non connection
59	BUZZER	I	BEEP FOR SW OPERATION
60	NC	-	Non connection
61	NC	-	Non connection
62	NC	-	Non connection
63	NC	-	Non connection
64	NC	-	Non connection
65	NC	-	Non connection
66	NC	-	Non connection
67	NC	-	Non connection
68	NC	-	Non connection
69	LM0	O	CD MECHA DRIVER CONT.
70	LM1	O	CD MECHA DRIVER CONT.
71	BUCK	O	CD LSI COMMUNICATION LINE
72	CCE	O	CD LSI COMMUNICATION LINE
73	BUS0	I/O	CD LSI COMMUNICATION LINE
74	BUS1	I/O	CD LSI COMMUNICATION LINE
75	BUS2	I/O	CD LSI COMMUNICATION LINE
76	BUS3	I/O	CD LSI COMMUNICATION LINE
77	RST	O	CD LSI COMMUNICATION LINE
78	PS1	I	ACC DETECTION INPUT
79	PS2	I	MEMORY DETECTION
80	DETACH	I	DETACH DETECTION
81	NC	-	Non connection
82	GND1	-	MONO BY FORCE
83	MONO	O	SWITCHING SEEK & STOP
84	SEEK/STOP	O	BAND SW
85	FM/AM	O	OUTPUT L
86	DIMIN	I	ILM CONTROL
87	ANT	O	ANT COTROL
88	TEL MUTE	I	TEL MUTE IN
89	STAGE1	-	Non connection
90	STAGE2	-	Non connection
91	NC	-	Non connection
92	NC	-	Non connection
93	NC	-	Non connection
94	NC	-	Non connection
95	NC	-	Non connection
96	NC	-	Non connection
97	NC	-	Non connection
98	DIMMER	O	DIMMER CONTROL
99	VDDPORT	-	-
100	GNDPORT	-	-

■ BA3220FV-X(IC341/IC441) : Line Out Amp

1. Terminal layout

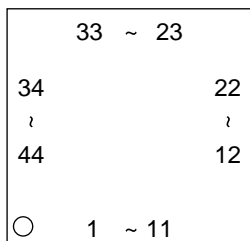


2. Block diagram

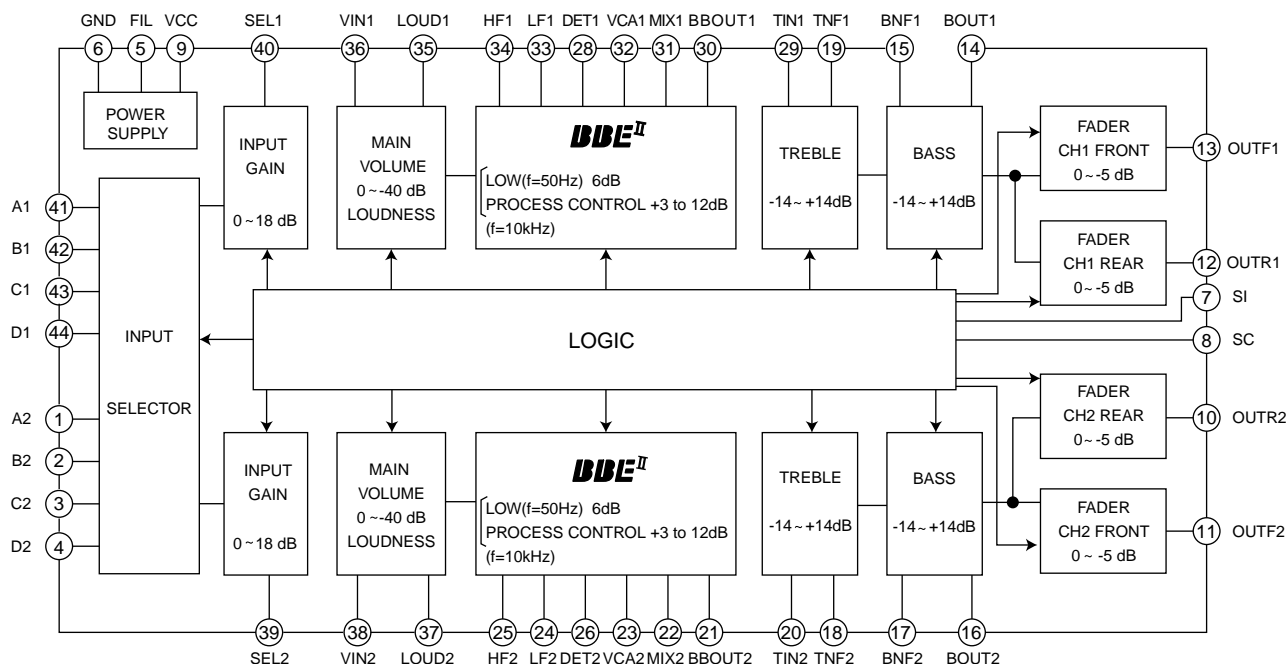


BD3860K (IC301):E.Volume

1. Terminal layout



2. Block diagram

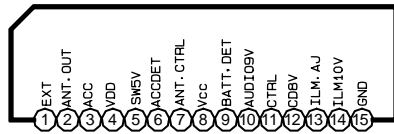


3. Pin function

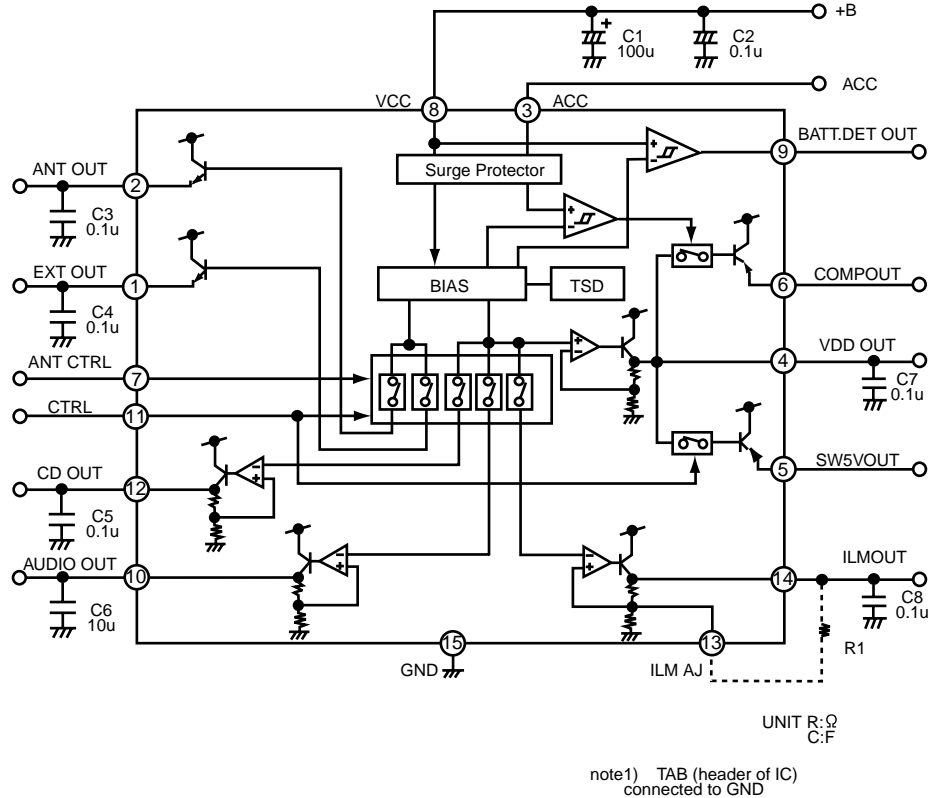
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	A2	CH2 Input Pin A	23	VCA2	CH2 High Pass VCA Output Pin
2	B2	CH2 Input Pin B	24	LF2	CH2 Low Pass Filter Setting Pin
3	C2	CH2 Input Pin C	25	HF2	CH2 High Pass Filter Setting Pin
4	D2	CH2 Input Pin D	26	DET2	CH2 High Pass Attack/Release Time Setting Pin
5	FIL	1/2 VCC Pin	27	NC	Non connect
6	GND	Ground Pin	28	DET1	CH1 High Pass Attack/Release Time Setting Pin
7	SI	Serial Data Receiving Pin	29	TIN1	CH1 treble Input Pin
8	SC	Serial Clock Receiving Pin	30	BBOUT1	CH1 BBE II Signal Output Pin
9	VCC	Power Supply Pin	31	MIX1	CH1 Output MIX Amplifier Inverse Input Pin
10	OUTR2	CH2 Rear Output Pin	32	VCA1	CH1 High Pass VCA Output Pin
11	OUTF2	CH2 Front Output Pin	33	LF1	CH1 Low Pass Filter Setting Pin
12	OUTR1	CH1 Rear Output Pin	34	HF1	CH1 High Pass Filter Setting Pin
13	OUTF1	CH1 Front Output Pin	35	LOUD1	CH1 Loudness Filter Setting Pin
14	BOUT1	CH1 Bass Filter Setting Pin	36	VIN1	CH1 Main Volume Input Pin
15	BNF1	CH1 Bass Filter Setting Pin	37	LOUD2	VCH2 Loudness Filter setting Pin
16	BOUT2	CH2 Bass Filter Setting Pin	38	VIN2	CH2 Main Volume Input Pin
17	BNF2	CH2 Bass Filter Setting Pin	39	SEL2	CH2 Input Gain Output Pin
18	TNF2	CH2 treble Filter Setting Pin	40	SEL1	CH1 Input Gain output Pin
19	TNF1	CH1 treble Filter Setting Pin	41	A1	CH1 Input Pin A
20	TIN2	CH2 treble Input Pin	42	B1	CH1 Input Pin B
21	BBOUT2	CH2 BBE II Signal Output Pin	43	C1	CH1 Input Pin C
22	MIX2	CH2 Output MIX Amplifier Inverse Input Pin	44	D1	CH1 Input Pin D

HA13164(IC961):REGULATOR

1.Terminal layout



2.Block diagram

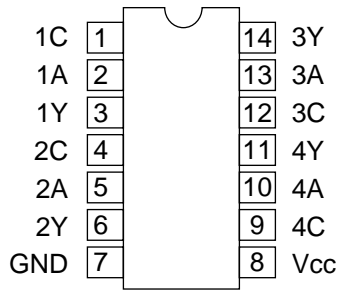


3.Pin function

Pin No.	Symbol	Function
1	EXTOUT	Output voltage is VCC-1 V when M or H level applied to CTRL pin.
2	ANTOUT	Output voltage is VCC-1 V when M or H level to CTRL pin and H level to ANT-CTRL.
3	ACCIN	Connected to ACC.
4	VDDOUT	Regular 5.7V.
5	SW5VOUT	Output voltage is 5V when M or H level applies to CTRL pin.
6	COMPOUT	Output for ACC detector.
7	ANT CTRL	L:ANT output OFF , H:ANT output ON
8	VCC	Connected to VCC.
9	BATT DET	Low battery detect.
10	AUDIO OUT	Output voltage is 9V when M or H level applied to CTRL pin.
11	CTRL	L:BIAS OFF, M:BIAS ON, H:CD ON
12	CD OUT	Output voltage is 8V when H level applied to CTRL pin.
13	ILM AJ	Adjustment pin for ILM output voltage.
14	ILM OUT	Output voltage is 10V when M or H level applies to CTRL pin.
15	GND	Connected to GND.

■ HD74HC126FP-X (IC771) : Buffer

1. Terminal layout

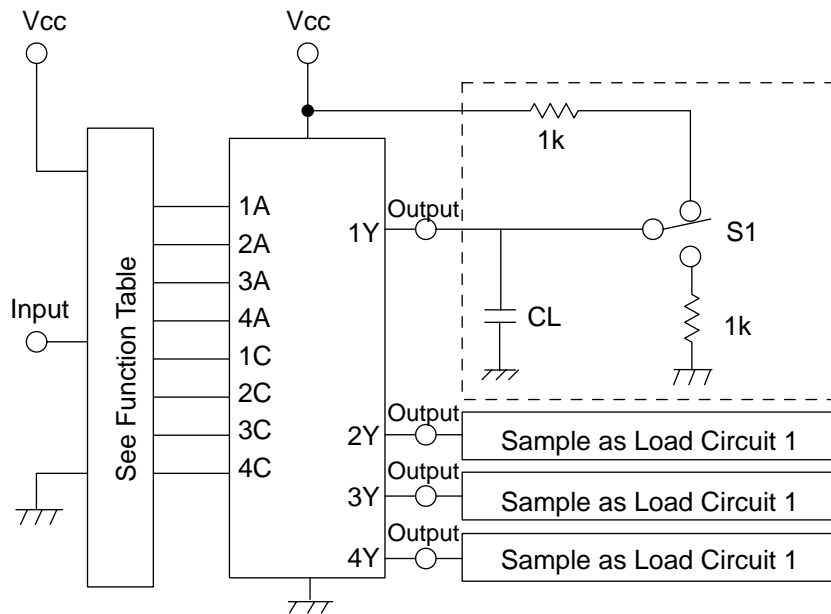


3. Pin function

Input		Output
C	A	Y
L	X	Z
H	L	H
H	H	L

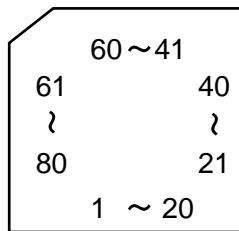
Note: H : High
 L : Low
 X : H and L
 Z : H.L.X

2. Block diagram

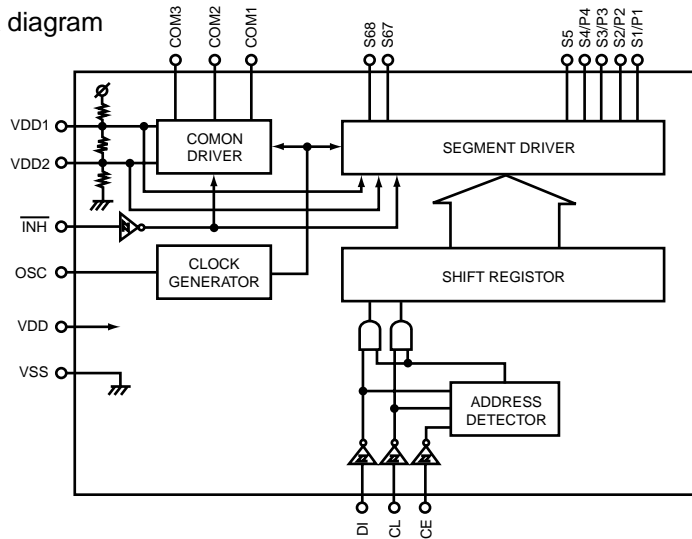


■ LC75873NW(IC601):LCD Driver

1.Pin layout



2.Block diagram

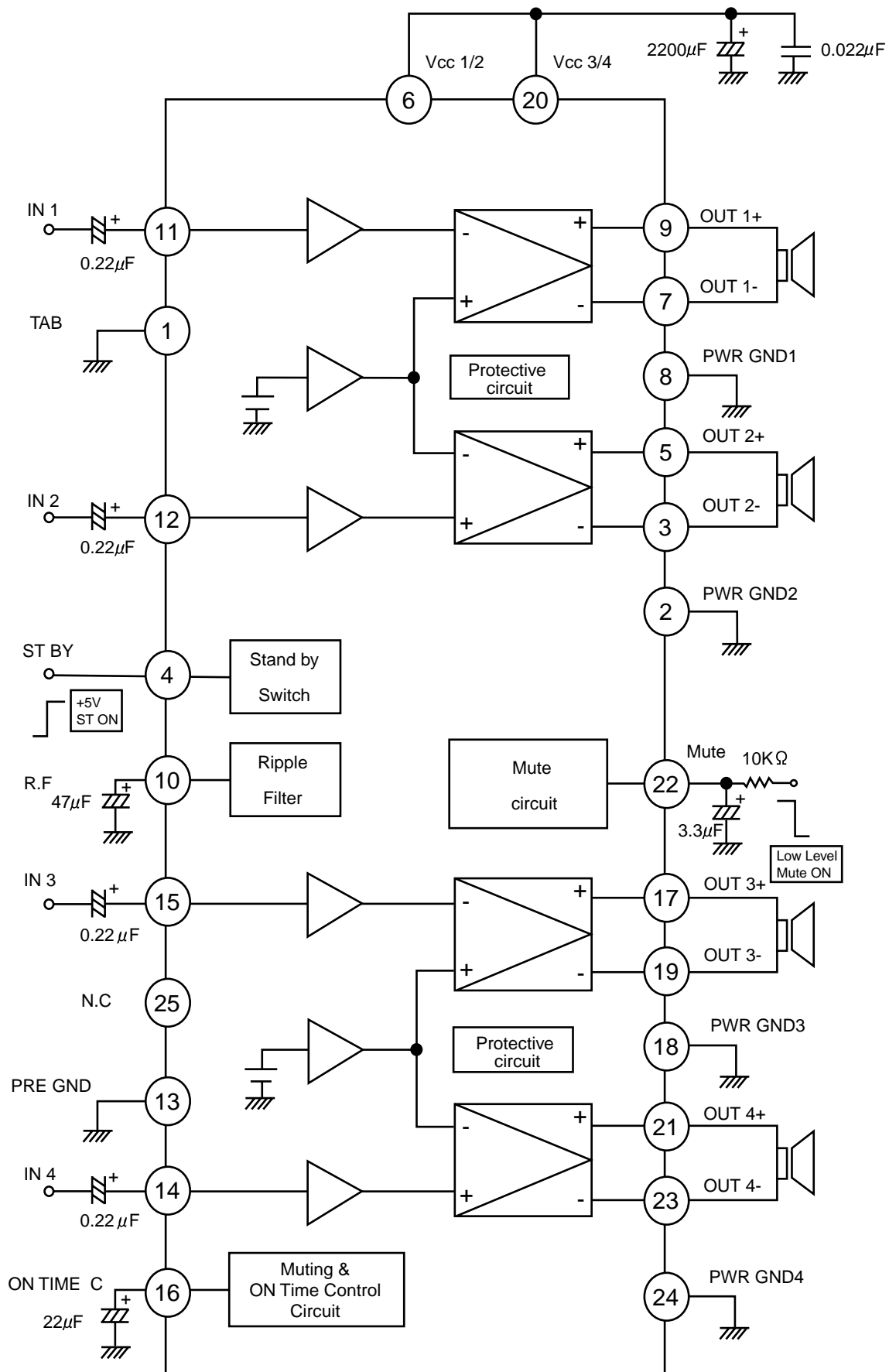


3.Pin function

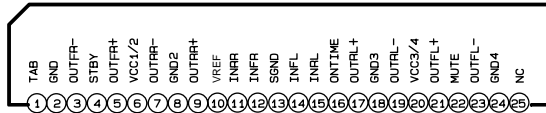
Pin No.	Pin name	I/O	Description
79,80 1,2,3 to 66	S1/P1 TO S4/P4 S5 to S68	O	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.
67 78 69	COM1 COM2 COM3	O	Common driver outputs. The frame frequency f_0 is given by : $f_0 = (FOSC/384)Hz.$
74	OSC	I/O	Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor to this pin.
76 77 78	CE CL DI	I	Serial data transfer inputs. Connected to the controller. CE:Chip enable CL:Synchronization clock DI:Transfer data
75	\overline{INH}	I	<u>Display off control input</u> <ul style="list-style-type: none"> $\overline{INH} = "L"(VSS)$... Display forced off S1/P1 to S4/P4 = "L" (These pins are forcibly set to the segment output port function and held at the low level.) S5 to S68 = "L" COM1 to COM3 "L" $\overline{INH} = "H"(HDD)$... Display on However, serial data transfer is possible when the display is forced off by this pin.
71	VDD1	I	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to VDD2 when a 1/2 bias drive scheme is used.
72	VDD2	I	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to VDD1 when a 1/2 bias drive scheme is used.
70	VDD	-	Power supply connection. Provide a voltage of between 3.0 and 6.0V.
73	VSS	-	Power supply connection. Connect to ground.

■ LA4743K(IC351):Power AMP

1.Block diagram



2. Terminal layout



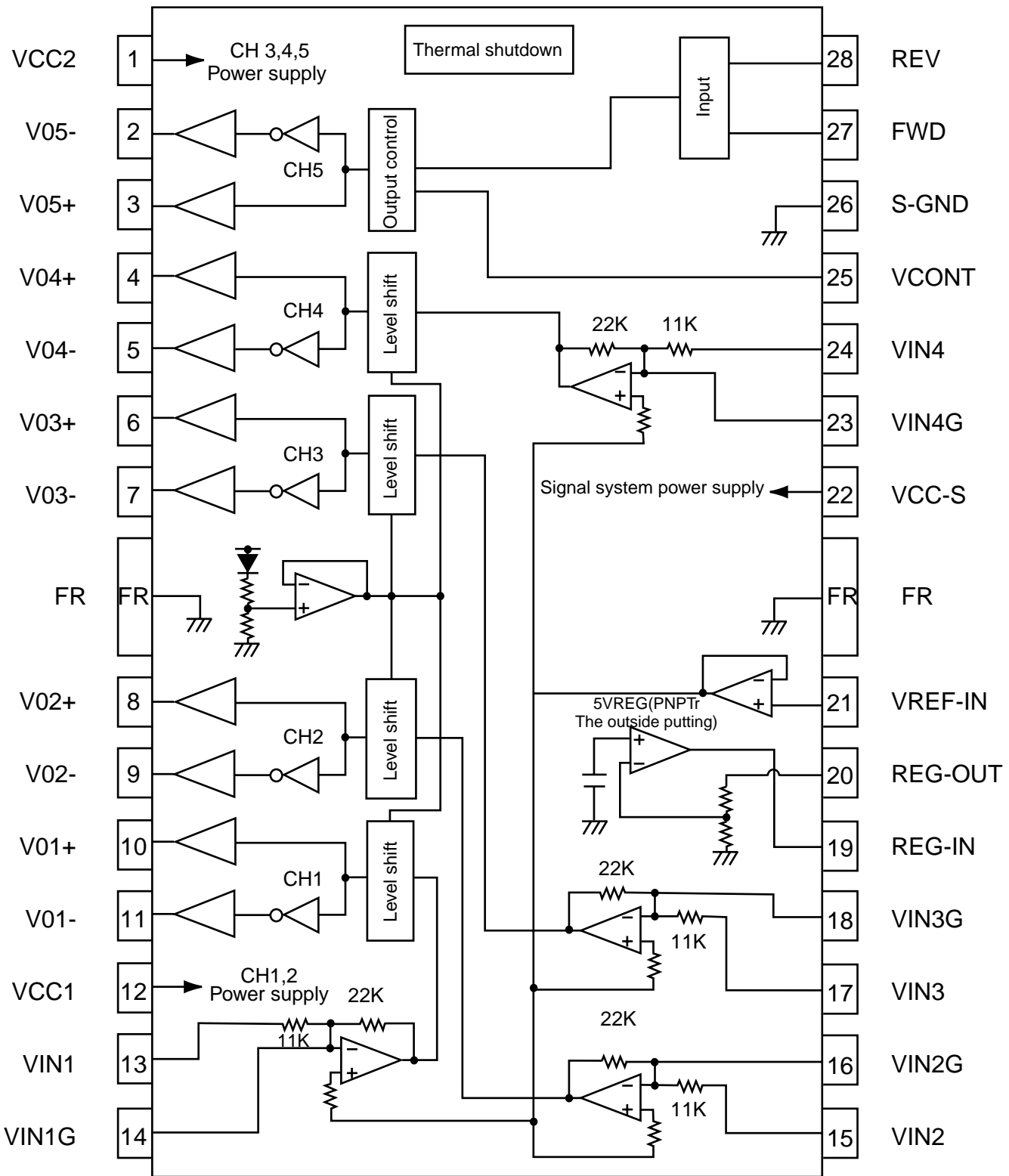
3. Pin function

LA4743K

Pin No.	Symbol	Function
1	TAB	Header of IC
2	GND	Power GND
3	OUTFR-	Output (-) for front Rch
4	STBY	Stand by input
5	OUTFR+	Output (+) for front Rch
6	VCC1/2	Power input
7	OUTRR-	Output (-) for rear Rch
8	GND	Power GND
9	OUTRR+	Output (+) for rear Rch
10	VREF	Ripple filter
11	INRR	Rear Rch input
12	INFR	Front Rch input
13	SGND	Signal GND
14	INFL	Front Lch input
15	INRL	Rear Lch input
16	ONTIME	Power on time control
17	OUTRL+	Output (+) for rear Lch
18	GND3	Power GND
19	OUTRL-	Output (-) for rear Lch
20	VCC3/4	Power input
21	OUTFL+	Output (+) for front
22	MUTE	Muting control input
23	OUTFL-	Output (-) for front
24	GND4	Power GND
25	NC	Non connection

■ LA6567H-X(IC581):CD DRIVER

1.Pin layout & blockdiagram



2. Pin function

LA6567H-X(2/2)

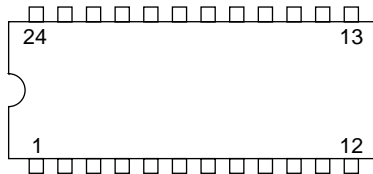
Pin no.	Symbol	Function
1	VCC2	CH3,4,5 Power supply(It is short with VCC1,VCC-S)
2	V05-	Loading output(-)
3	V05+	Loading terminal (+)
4	V04+	CH4 Output terminal(+)
5	V04-	CH4 Output terminal(-)
6	V03+	CH3 Output terminal(+)
7	V03-	CH3 Output terminal(-)
8	V02+	CH2 Output terminal(+)
9	V02-	CH2 Output terminal(-)
10	V01+	CH1 Output terminal(+)
11	V01-	CH1 Output terminal(-)
12	VCC1	CH1,2(BTL) Power supply(It is short with VCC-S,VCC2)
13	VIN1	CH1 Input terminal
14	VIN1G	CH1 Input terminal(For gain adjustment)
15	VIN2	CH2 Input terminal
16	VIN2G	CH2 Input terminal(For gain adjustment)
17	VIN3	CH3 Input terminal
18	VIN3G	CH3 Input terminal(For gain adjustment)
19	REG-IN	Regulator terminal(Outside putting PNP base)
20	REG-OUT	Regulator terminal(Outside putting PNP collector)
21	VREF-IN	Standard voltage input terminal
22	VCC-S	Signal system power supply(It is short with VCC1,VCC2)
23	VIN4G	CH4 Input terminal(For gain adjustment)
24	VIN4	CH4 Input terminal
25	VCONT	5CH(VLO) Output voltage set terminal
26	S-GND	Signal system GND
27	FWD	5CH(VLO)Signal output switch terminal(FWD),Input of logic of loading part
28	REV	5CH(VLO)Signal output switch terminal(REV), Input of logic of loading part

* Frame(FR)at the center becomes system GND.

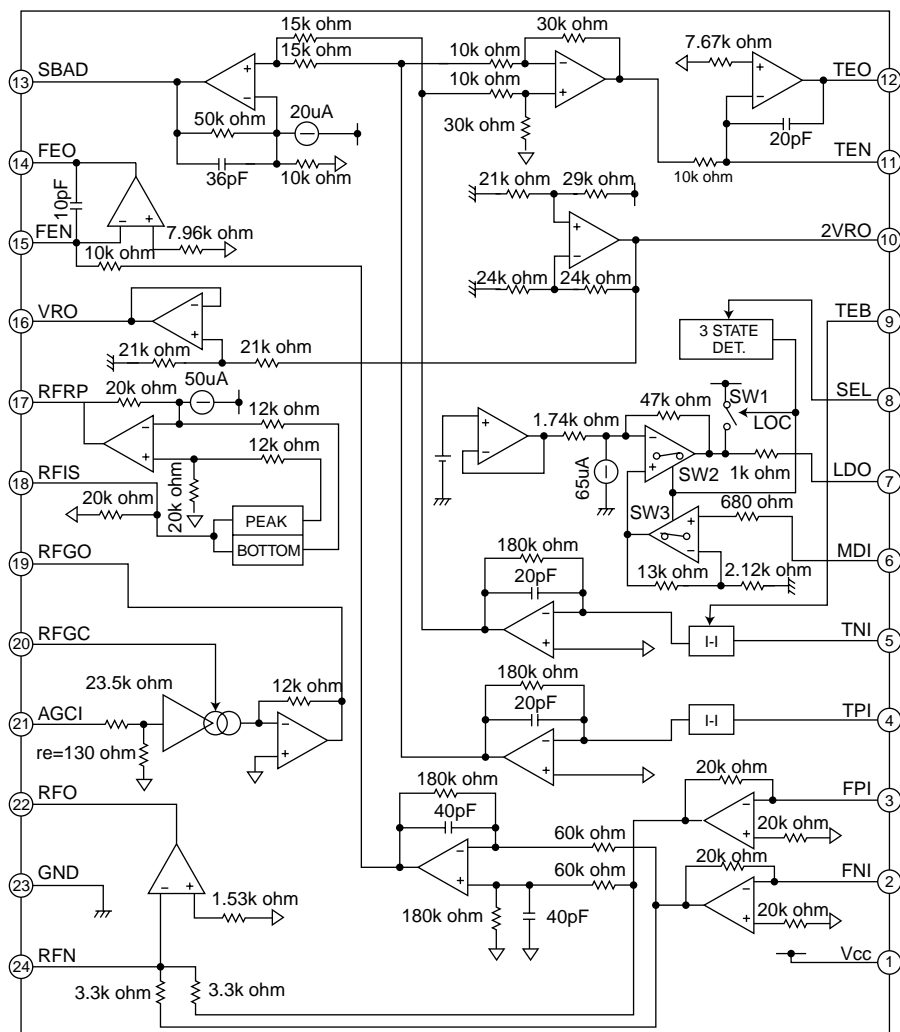
* Please be short-circuited on the outside and use the terminal of the power supply system and three terminals of VCC-S, VCC1,VCC2.

■ TA2109F-X (IC501) : RF amp.

1. Pin layout



2. Block diagram

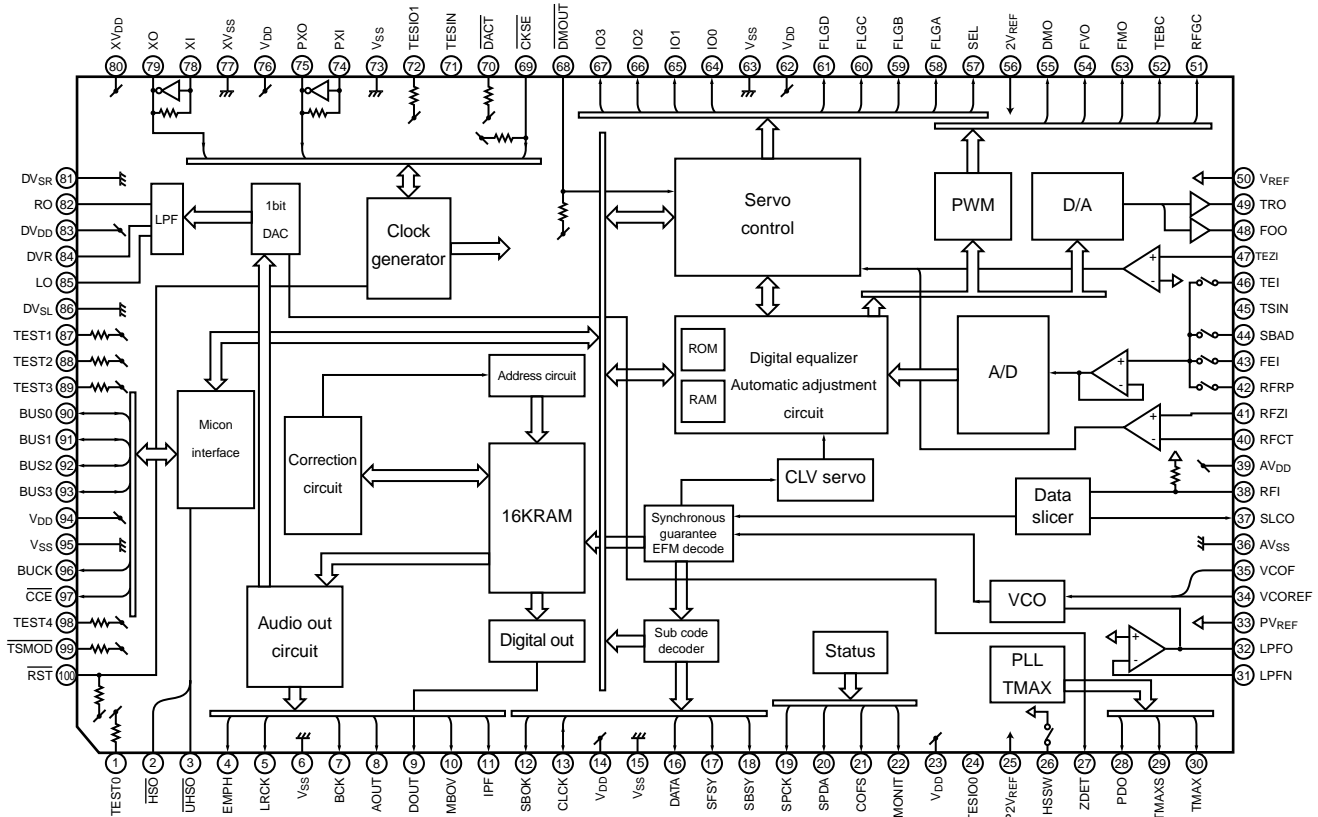


3. Pin function

Pin No.	Symbol	I/O	Pin function	Pin No.	Symbol	I/O	Pin function
1	Vcc	-	Power supply input terminal	13	SBAD	O	Sub beam adder signal output terminal
2	FNI	I	Main beam I-V amp input terminal	14	FEO	O	Focus error signal output terminal
3	FPI	I	Main beam I-V amp input terminal	15	FEN	I	FE amp negative input terminal
4	TPI	I	Sub beam I-v input terminal	16	VRO	O	Reference voltage (VREF) output terminal
5	TNI	I	Sub beam I-V input terminal	17	RFRP	O	Track count signal output terminal
6	MDI	I	Monitor photo diode amp input terminal	18	RFIS	I	RFRP detect circuit input terminal
7	LDO	O	Laser diode amp output terminal	19	RFGO	O	RF gain signal output terminal
8	SEL	I	Laser diode control signal input terminal	20	RFGC	I	RF amplitude adj. control signal input terminal
9	TEB	I	T. error balance adj. signal input terminal	21	AGCI	I	RF signal amplitude adj. amp input terminal
10	2VRO	O	Reference voltage output terminal	22	RFO	O	RF signal output terminal
11	TEN	I	TE amp negative input terminal	23	GND	-	Ground terminal
12	TEO	O	TE error signal output terminal	24	RFN	I	RF amp negative input terminal

TC9462F(IC521):

1.Pin layout & Block Diagram



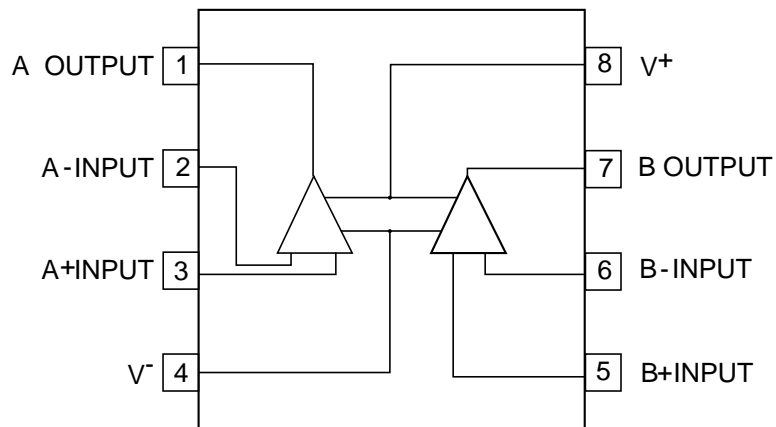
2.Pin function

PIN No.	SYMBOL	I/O	FUNCTIONAL DESCRIPTION	REMARKS															
1	TEST0	I	Test mode terminal. Normally, Keep at open.	With pull-up resistor.															
2	HSO	O	Playback speed mode flag output terminal. <table border="1" style="margin-left: 20px;"> <tr> <th>UHSO</th> <th>HSO</th> <th>PLAYBACK SPEED</th> </tr> <tr> <td>H</td> <td>H</td> <td>Nomal</td> </tr> <tr> <td>H</td> <td>L</td> <td>2 times</td> </tr> <tr> <td>L</td> <td>H</td> <td>4 times</td> </tr> <tr> <td>L</td> <td>L</td> <td>--</td> </tr> </table>	UHSO	HSO	PLAYBACK SPEED	H	H	Nomal	H	L	2 times	L	H	4 times	L	L	--	--
UHSO	HSO	PLAYBACK SPEED																	
H	H	Nomal																	
H	L	2 times																	
L	H	4 times																	
L	L	--																	
3	UHSO	O																	
4	EMPH	O	Subcode Q data emphasis flag output terminal. Emphasis ON at "H" level and OFF at "L" level. The output polarity can invert by command.	--															
5	LRCK	O	Channel clock output terminal. (44.1kHz) L-ch at "L" level and R-ch at "H" level. the output polarity can invert by command.	--															
6	VSS	--	Digital GND terminal.	--															
7	BCK	O	Bit clock output terminal. (1.4112MHz)	--															
8	AOUT	O	Audio data output terminal.	--															
9	DOUT	O	Digital data output terminal.	--															
10	MBOV	O	Buffer memory over signal output terminal. Over at "H" level.	--															
11	IPF	O	Correction flag output terminal. At "H" level, AOUT output is made to correction impossibility by C2 correction processing.	--															
12	SBOK	O	Subcode Q data CRCC check adjusting result output terminal. The adjusting result is OK at "H" level.	--															
13	CLCK	I/O	Subcode P~W data readout clock input/output terminal. This terminal can select by command bit.	--															
14	VDD	--	Digital power supply voltage terminal.	--															
15	VSS	--	Digital GND terminal.	--															
16	DATA	O	Subcode P~W data output terminal.	--															
17	SFSY	O	Play-back frame sync signal output terminal.	--															
18	SBSY	O	Subcode block sync signal output terminal.	--															
19	SPCK	O	Processor status signal readout clock output terminal.	--															
20	SADA	O	Processor status signal output terminal.	--															
21	COFS	O	Correction frame clock output terminal. (7.35kHz)	--															
22	MONIT	O	Internal signal (DSP internal flag and PLL clock) output terminal. Selected by command. This terminal output the text data with serial by command.	--															
23	VDD	--	Digital power supply voltage terminal.	--															
24	TESIO0	I	Test input/output terminal. Normally, keep at "L" level. The terminal that inputted the clock for read of text data by command.	--															
25	P2VREF	--	PLL double reference voltage supply terminal.	--															

Pin No.	Symbol	I/O	Function	Remarks								
26	HSSW	O	2/4 times speed at "VREF" voltage.	2-state output(PVREF,HIZ)								
27	ZDET	O	1 bit DA converter zero detect flag output terminal.	-								
28	PDO	O	Phase difference signal output terminal of EFM signal and PLCK signal.	3-state output. (P2VREF,PVREF,VSS)								
29	TMAXS	O	TMAX detection result output terminal. Selected by command bit (TMPS)	3-state output. (P2VREF,PVREF,VSS)								
30	TMAX	O	TMAX detection result output terminal. Selected by command bit (TMPS)	3-state output. (P2VREF,HIZ,VSS)								
			<table border="1"> <tr> <td>DIFFERENCE RESULT</td> <td>TMAX OUTPUT</td> </tr> <tr> <td>Longer than fixed freq.</td> <td>"P2VREF"</td> </tr> <tr> <td>Shorter than fixed freq.</td> <td>"VSS"</td> </tr> <tr> <td>Within the fixed freq.</td> <td>"Hiz"</td> </tr> </table>	DIFFERENCE RESULT	TMAX OUTPUT	Longer than fixed freq.	"P2VREF"	Shorter than fixed freq.	"VSS"	Within the fixed freq.	"Hiz"	
DIFFERENCE RESULT	TMAX OUTPUT											
Longer than fixed freq.	"P2VREF"											
Shorter than fixed freq.	"VSS"											
Within the fixed freq.	"Hiz"											
31	LPFN	I	LPF amplifier inverting terminal for PLL.	Analog input.								
32	LPFO	O	LPF amplifier output terminal for PLL.	Analog output.								
33	PVREF	-	PLL reference voltage supply terminal.	-								
34	VCOREF	I	VCO center frequency reference level terminal. Normally, keep at "PVREF" level.	-								
35	VCOF	O	VCO filter terminal.	Analog output.								
36	AVSS	-	Analog GND terminal.	-								
37	SLCO	O	Data slice level output terminal.	Analog output.								
38	RFI	I	RF signal input terminal.	Analog input. (Zin:selected by command)								
39	AVDD	-	Analog power supply voltage terminal.	-								
40	RFCT	I	RFRP signal center level input terminal	Analog input(Zin : 50k Ω)								
41	RFZI	I	RFRP zero cross input terminal	Analog input.								
42	RFRP	I	RF ripple signal input terminal	Analog input.								
43	FEI	I	Focus error signal input terminal	Analog input.								
44	SBAD	I	Sub-beam adder signal input terminal	Analog input.								
45	TSIN	I	Test input terminal Normally, keep at "vref" level	Analog input.								
46	TEI	I	Tracking error signal input terminal. Take in at tracking servo ON.	Analog input.								
47	TEZI	I	Tracking error zero cross input terminal	Analog input(Zin :10k Ω)								
48	FOO	O	Focus servo equalizer output terminal	Analog output.(2VREF-AVSS)								
49	TRO	O	Tracking servo equalizer output terminal	-								
50	VREF	-	Analog reference voltage supply terminal	3-state PWM signal output.								
51	RFGC	O	RF amplitude adjustment control signal output terminal	(2VREF,VREF,VSS)								
52	TEBC	O	Tracking balance control signal output terminal	(PWM carrier =88.2kHz)								
53	FMO	O	Feed equalizer output terminal									
54	FVO	O	Speed error signal or feed search equalizer output terminal									
55	DMO	O	Disk equalizer output terminal (PWM carrier=88.2kHz for DSP, Synchronize to PXO)	3-state output. (2VREF,VREF,VSS)								
56	2VREF	-	Analog double reference voltage supply terminal	-								
57	SEL	O	APC circuit ON/OFF indication signal output terminal	-								
58~61	FLGA~D	O	External flag output terminal for internal signal	-								
62	VDD	-	Digital power supply voltage terminal	-								
63	VSS	-	Digital GND terminal	-								
64~67	IO0~3	I/O	General I/O terminal	-								
68	DMOUT	I	This terminal control IO0~IO3 terminal	With pull-up resistor.								
69	CKSE	I	Normally, keep at open	With pull-up resistor.								
70	DACT	I	DAC test mode terminal. Normally, keep at open	With pull-up resistor.								

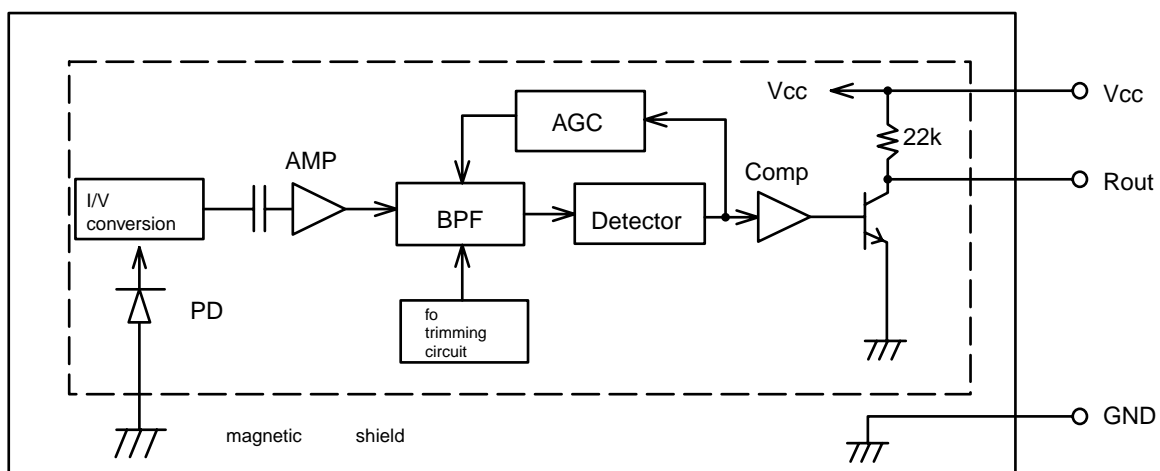
Pin No.	Symbol	I/O	Function	Remarks
71	TESIN	I	Test input terminal, Normally, keep at "L" level	Analog input.
72	TESIO1	I	Test input/output terminal. Normally, keep at "L" level	Analog input.
73	VSS	-	Digital GND terminal	-
74	PXI	I	Crystal oscillator connecting input terminal for DSP	-
75	PXO	O	Crystal oscillator connecting output terminal for DSP	-
76	VDD	-	Digital power supply voltage terminal	-
77	XVSS	-	Oscillator GND terminal for system clock	-
78	XI	I	Crystal oscillator connecting input terminal for system clock	-
79	XO	O	Crystal oscillator connecting output terminal for system clock	-
80	XVDD	-	Oscillator power supply voltage terminal for system clock	-
81	DVSR	-	Analog GND terminal for DA converter (Rch)	-
82	RO	O	R channel data forward output terminal	-
83	DVDD	-	Analog supply voltage terminal for DA converter	-
84	DVR	-	Reference voltage terminal for DA converter	-
85	LO	O	L channel data forward output terminal	-
86	DVSL	-	Analog GND terminal for DA converter (Lch)	-
87~89	TEST1~3	I	Test mode terminal . Normal keep at open	With piull-up resistor.
90~93	BUS0~3	I/O	Micon interface data input/output terminal	Schmit input. With pull-up resistor.
94	VDD	-	Digital power supply voltage terminal	-
95	VSS	-	Digital GND terminal	-
96	BUCK	I	Micon interface clock input terminal	Schmit input.
97	CCE	I	Command and data sending/receiving chip enable signal input terminal	Schmit input.
98	TEST4	I	Test mode terminal. Normal, keep at open	With pull-up resistor.
99	TSMOD	I	Local test mode selection terminal	With pull-up resistor.
100	RST	I	Reset signal input terminal. Reset at "L" level	With pull-up resistor.

■ NJM4565M-WE (IC111) : Ope. amp



■ RPM6938-SV4(IC602) : Remote Censor

1. Block diagram





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